



# SPEC CPU®2017 Integer Rate Result

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## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4216, 2.10GHz)

SPECrate®2017\_int\_base = 178

SPECrate®2017\_int\_peak = 186

CPU2017 License: 9019

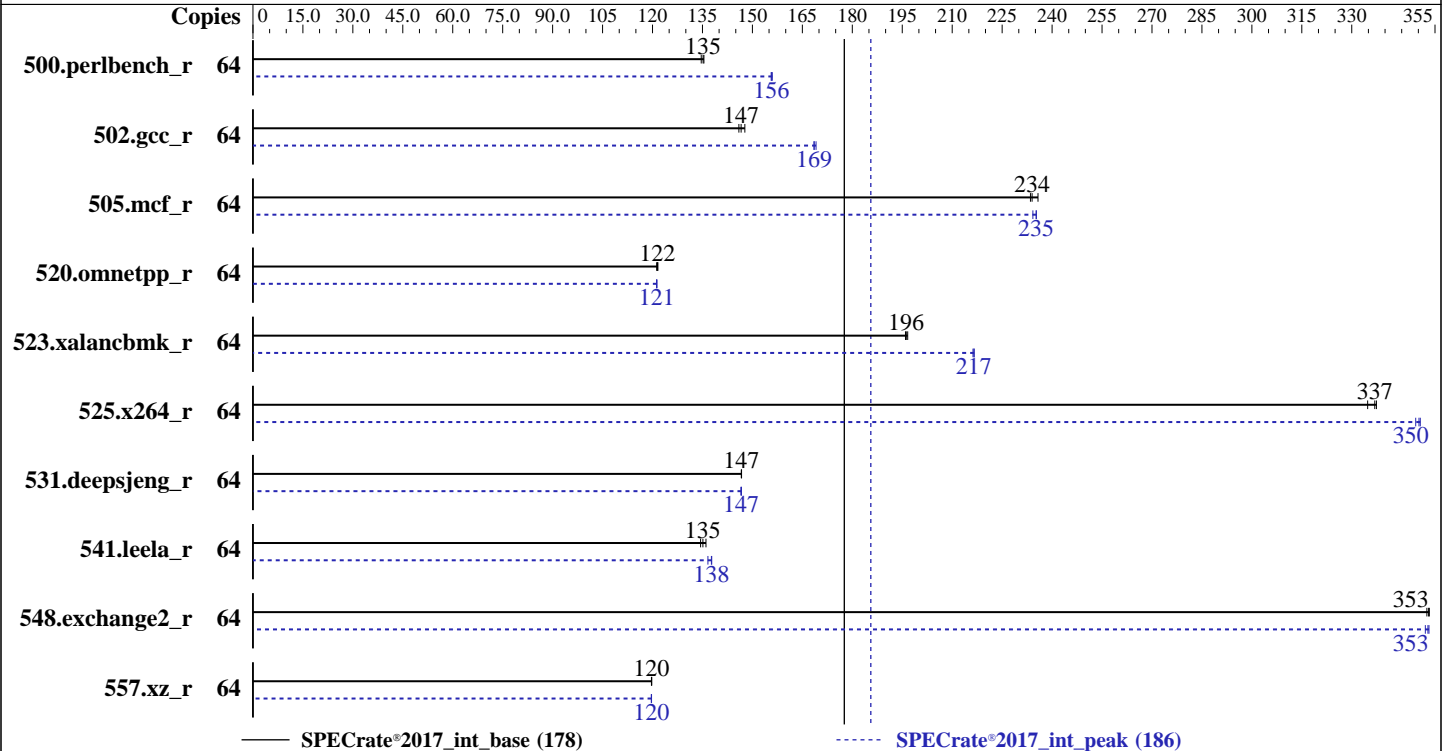
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Silver 4216  
 Max MHz: 3200  
 Nominal: 2100  
 Enabled: 32 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 22 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4d released May-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 32/64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: --



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	64	757	135	<b>754</b>	<b>135</b>	752	135	64	653	156	655	156	<b>654</b>	<b>156</b>
502.gcc_r	64	<b>618</b>	<b>147</b>	613	148	621	146	64	<b>538</b>	<b>169</b>	538	168	536	169
505.mcf_r	64	<b>442</b>	<b>234</b>	443	234	439	236	64	442	234	<b>440</b>	<b>235</b>	440	235
520.omnetpp_r	64	693	121	<b>691</b>	<b>122</b>	690	122	64	693	121	<b>692</b>	<b>121</b>	692	121
523.xalancbmk_r	64	<b>344</b>	<b>196</b>	345	196	344	197	64	<b>312</b>	<b>217</b>	313	216	312	217
525.x264_r	64	<b>333</b>	<b>337</b>	335	335	332	337	64	321	349	320	351	<b>320</b>	<b>350</b>
531.deepsjeng_r	64	500	147	<b>500</b>	<b>147</b>	500	147	64	<b>500</b>	<b>147</b>	500	147	500	147
541.leela_r	64	<b>784</b>	<b>135</b>	779	136	788	134	64	776	137	<b>770</b>	<b>138</b>	769	138
548.exchange2_r	64	<b>475</b>	<b>353</b>	475	353	476	353	64	475	353	<b>475</b>	<b>353</b>	476	352
557.xz_r	64	<b>577</b>	<b>120</b>	578	120	577	120	64	<b>578</b>	<b>120</b>	578	120	577	120

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop\_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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### General Notes (Continued)

is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-4vt5 Sat Aug 3 08:04:15 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
 2 "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores     : 16
  siblings      : 32
 physical 0:    cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
 physical 1:    cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s):       2
NUMA node(s):   4
Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping:        6
```

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### Platform Notes (Continued)

```

CPU MHz: 2100.000
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bml hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 22528 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 192103 MB
node 0 free: 191677 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 193498 MB
node 1 free: 193173 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 193527 MB
node 2 free: 193230 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 193526 MB
node 3 free: 193285 MB
node distances:
node  0  1  2  3
0:  10  11  21  21
1:  11  10  21  21

```

(Continued on next page)



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### Platform Notes (Continued)

```
2: 21 21 10 11
3: 21 21 11 10
```

```
From /proc/meminfo
MemTotal:      791200216 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-4vt5 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation,
IBPB, IBRS_FW
```

```
run-level 3 Aug 3 02:40
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   224G   20G  204G   9% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400
```

(End of data from sysinfo program)



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### Compiler Version Notes

=====  
C | 502.gcc\_r(peak)  
-----

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 502.gcc\_r(peak)  
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Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 523.xalanbmk\_r(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalanbmk\_r(base)  
531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,

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## Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++ | 523.xalancbmk\_r(peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)  
| 531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
Fortran | 548.exchange2\_r(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

C++ benchmarks:  
icpc -m64

Fortran benchmarks:  
ifort -m64

## Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

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## Base Portability Flags (Continued)

```
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

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## Peak Compiler Invocation (Continued)

Fortran benchmarks:

ifort -m64

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r
```

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## Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

523.xalancbmk\_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

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Tested with SPEC CPU®2017 v1.0.5 on 2019-08-02 22:34:14-0400.

Report generated on 2020-07-01 19:06:52 by CPU2017 PDF formatter v6255.

Originally published on 2019-08-20.