SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

$SPECspeed®2017\_fp\_base =$ 40.2

$SPECspeed®2017\_fp\_peak =$ Not Run
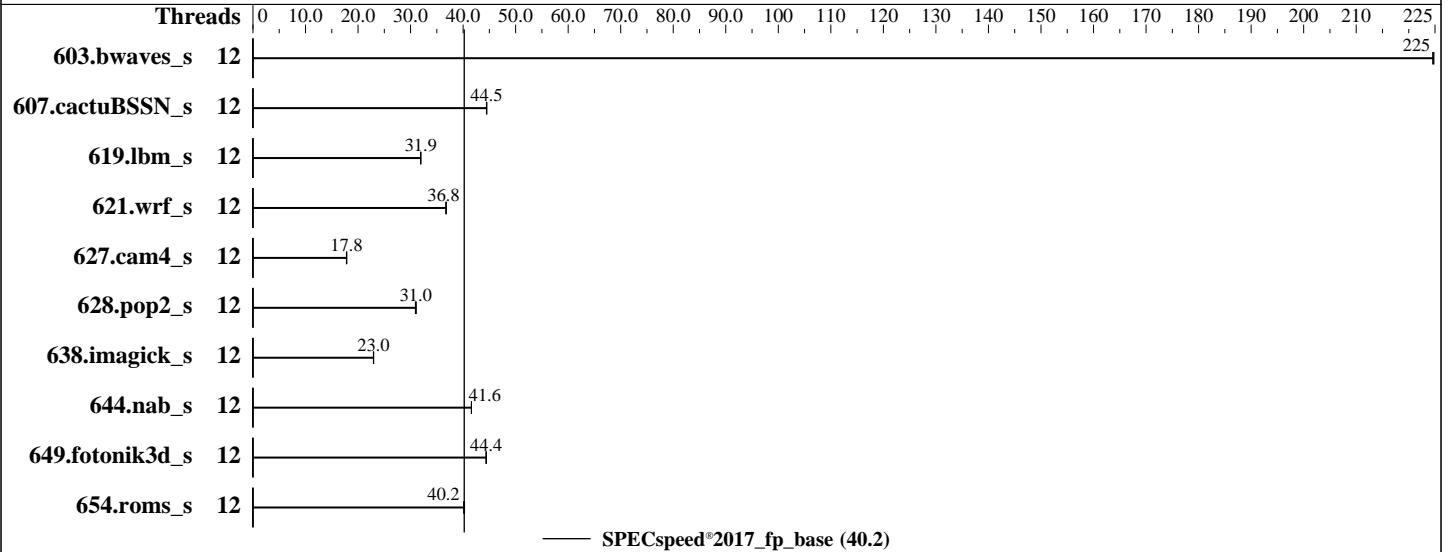
CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Threads | 0   10.0   20.0   30.0   40.0   50.0   60.0   70.0   80.0   90.0   100   110   120   130   140   150   160   170   180   190   200   210   225

603.bwaves_s   12   225

607.cactuBSSN_s   12   44.5

619.lbm_s   12   31.9

621.wrf_s   12   36.8

627.cam4_s   12   17.8

628.pop2_s   12   31.0

638.imagick_s   12   23.0

644.nab_s   12   41.6

649.fotonik3d_s   12   44.4

654.roms_s   12   40.2

—— **SPECspeed®2017_fp_base (40.2)**

Hardware

CPU Name: Intel Xeon Bronze 3104
 Max MHz: 1700
 Nominal: 1700
Enabled: 12 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 8.25 MB I+D on chip per chip
 Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2133)
Storage: 1 x 600G SAS 10K RPM
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.1 released Oct-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --

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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	12	262	225	**263**	**225**	263	225							
607.cactuBSSN_s	12	**375**	**44.5**	375	44.4	374	44.5							
619.lbm_s	12	164	32.0	**164**	**31.9**	164	31.9							
621.wrf_s	12	**360**	**36.8**	360	36.7	359	36.8							
627.cam4_s	12	498	17.8	**497**	**17.8**	496	17.9							
628.pop2_s	12	**383**	**31.0**	382	31.1	384	30.9							
638.imagick_s	12	**628**	**23.0**	629	22.9	628	23.0							
644.nab_s	12	420	41.6	**420**	**41.6**	420	41.6							
649.fotonik3d_s	12	205	44.4	**205**	**44.4**	205	44.4							
654.roms_s	12	391	40.3	**392**	**40.2**	393	40.1							
SPECspeed®2017_fp_base =		**40.2**												
SPECspeed®2017_fp_peak =		**Not Run**												

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

 Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.4
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>   /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

CPU performance set to Enterprise

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Platform Notes (Continued)

```
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-fdny Wed Dec 12 21:57:20 2018

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
       2  "physical id"s (chips)
       12 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 6
       siblings  : 6
       physical 0: cores 0 1 2 3 4 5
       physical 1: cores 0 1 2 3 4 5

 From lscpu:
       Architecture:         x86_64
       CPU op-mode(s):       32-bit, 64-bit
       Byte Order:           Little Endian
       CPU(s):               12
       On-line CPU(s) list:  0-11
       Thread(s) per core:   1
       Core(s) per socket:   6
       Socket(s):            2
       NUMA node(s):         2
       Vendor ID:            GenuineIntel
       CPU family:           6
       Model:                85
       Model name:           Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
       Stepping:             4
       CPU MHz:              1437.638
       CPU max MHz:          1700.0000
       CPU min MHz:          800.0000
       BogoMIPS:             3392.02
       Virtualization:       VT-x
       L1d cache:            32K
       L1i cache:            32K
       L2 cache:             1024K
       L3 cache:             8448K
       NUMA node0 CPU(s):    0-5
```

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Test Date: Dec-2018
Hardware Availability: Aug-2017
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Platform Notes (Continued)

```
     NUMA node1 CPU(s):     6-11
     Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
   pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
   lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
   aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
   fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
   xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb invpcid_single pln pts
   dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
   retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
   avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
   clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 8448 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5
   node 0 size: 385626 MB
   node 0 free: 379840 MB
   node 1 cpus: 6 7 8 9 10 11
   node 1 size: 387054 MB
   node 1 free: 384955 MB
   node distances:
   node   0   1
     0:  10  21
     1:  21  10

 From /proc/meminfo
    MemTotal:       791225708 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 2
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
    os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
```

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Platform Notes (Continued)

```
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-fdny 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Dec 12 11:18

 SPEC is set to: /home/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sda2       xfs   500G  168G  333G  34% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
   Memory:
    24x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2133

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                     | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran               | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
```

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Test Sponsor: Cisco Systems	**Hardware Availability:** Aug-2017
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Compiler Version Notes (Continued)

```
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
Fortran, C    | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

603.bwaves_s: `-DSPEC_LP64`
607.cactuBSSN_s: `-DSPEC_LP64`
619.lbm_s: `-DSPEC_LP64`
621.wrf_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
627.cam4_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
628.pop2_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
638.imagick_s: `-DSPEC_LP64`
644.nab_s: `-DSPEC_LP64`
649.fotonik3d_s: `-DSPEC_LP64`
654.roms_s: `-DSPEC_LP64`

https://www.spec.org/

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Tested by:	Cisco Systems	**Software Availability:**	Oct-2018

Base Optimization Flags

C benchmarks:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:
```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using Fortran, C, and C++:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

---

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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