SPEC® CPU2017 Floating Point Rate Result

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECrate2017_fp_base = 364

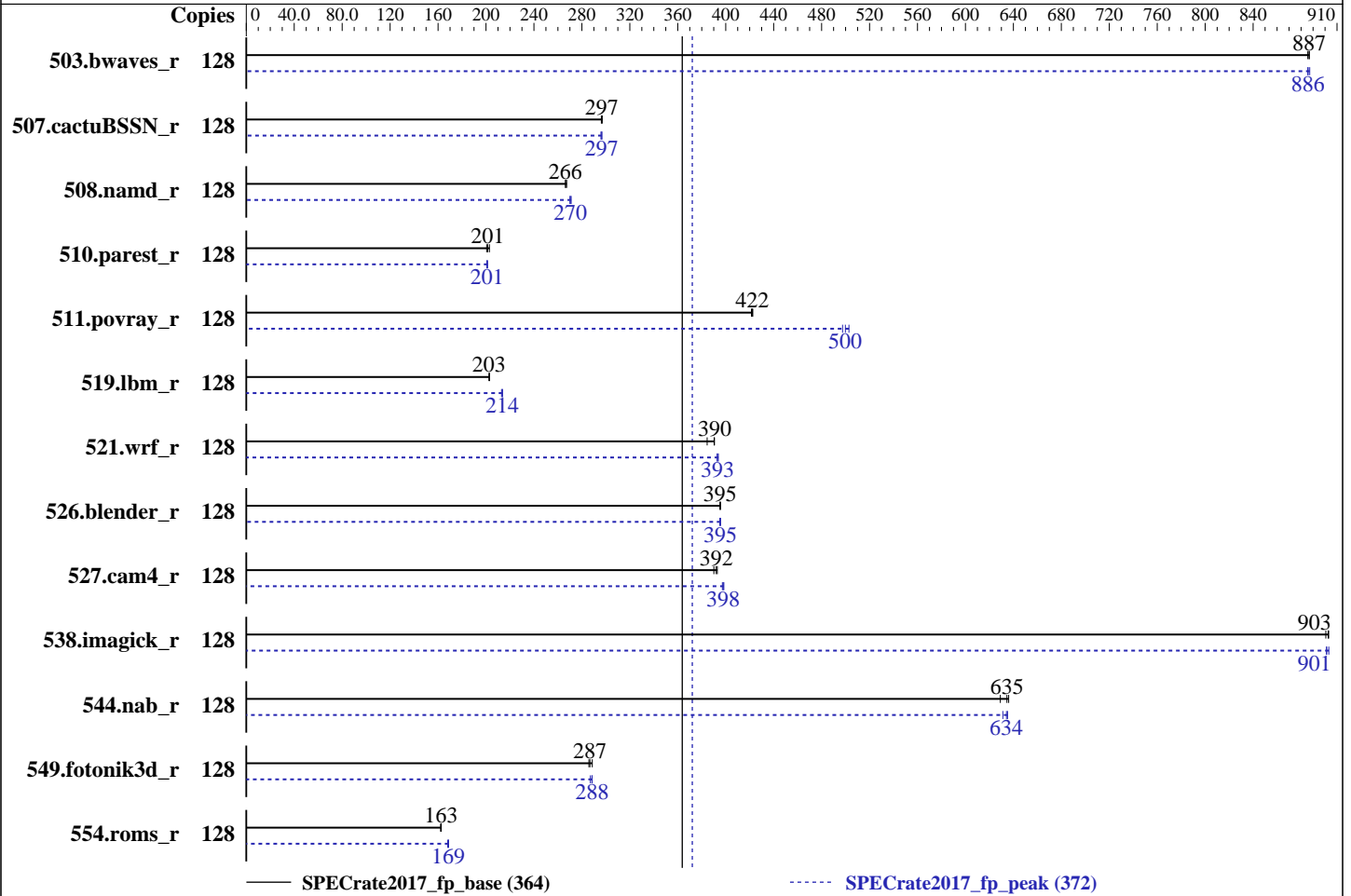SPECrate2017_fp_peak = 372

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Copies	Base	Peak
503.bwaves_r 128	887	886
507.cactuBSSN_r 128	297	297
508.namd_r 128	266	270
510.parest_r 128	201	201
511.povray_r 128	422	500
519.lbm_r 128	203	214
521.wrf_r 128	390	393
526.blender_r 128	395	395
527.cam4_r 128	392	398
538.imagick_r 128	903	901
544.nab_r 128	635	634
549.fotonik3d_r 128	287	288
554.roms_r 128	163	169

SPECrate2017_fp_base (364)   SPECrate2017_fp_peak (372)

Hardware

CPU Name: Intel Xeon Gold 6142M
 Max MHz.: 3700
 Nominal: 2600
Enabled: 64 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 22 MB I+D on chip per chip
 Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
 4.4.103-92.56-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 18.0.2.199 of Intel Fortran
 Compiler for Linux
Parallel: No
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None

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SPEC CPU2017 Floating Point Rate Result

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CPU2017 License: 9019	**Test Date:** Nov-2018
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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	128	**1448**	**887**	1449	886	1447	887	128	1447	887	1449	886	**1449**	**886**
507.cactuBSSN_r	128	**546**	**297**	547	296	546	297	128	**546**	**297**	546	297	548	296
508.namd_r	128	**457**	**266**	455	267	457	266	128	**450**	**270**	450	270	449	271
510.parest_r	128	1651	203	1670	201	**1662**	**201**	128	1663	201	**1666**	**201**	1669	201
511.povray_r	128	**708**	**422**	707	423	709	421	128	601	497	594	503	**598**	**500**
519.lbm_r	128	**666**	**203**	666	203	665	203	128	**631**	**214**	633	213	631	214
521.wrf_r	128	734	391	**735**	**390**	746	384	128	**729**	**393**	730	393	728	394
526.blender_r	128	**493**	**395**	493	395	493	396	128	**493**	**395**	493	395	493	396
527.cam4_r	128	570	393	**571**	**392**	574	390	128	564	397	**563**	**398**	562	398
538.imagick_r	128	353	903	**353**	**903**	353	901	128	**353**	**901**	352	903	353	901
544.nab_r	128	339	636	**339**	**635**	342	629	128	341	631	339	635	**340**	**634**
549.fotonik3d_r	128	**1740**	**287**	1745	286	1728	289	128	**1729**	**288**	1738	287	1729	288
554.roms_r	128	**1251**	**163**	1255	162	1250	163	128	1210	168	1205	169	**1206**	**169**

SPECrate2017_fp_base =	**364**
SPECrate2017_fp_peak =	**372**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)

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SPEC CPU2017 Floating Point Rate Result

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Cisco Systems

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SPECrate2017_fp_base =   364

SPECrate2017_fp_peak =   372

General Notes (Continued)

```
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /opt/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-vb5q Mon Nov  5 18:31:15 2018

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
       4  "physical id"s (chips)
       128 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 16
       siblings  : 32
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

 From lscpu:
       Architecture:          x86_64
       CPU op-mode(s):        32-bit, 64-bit
       Byte Order:            Little Endian
       CPU(s):                128
       On-line CPU(s) list:   0-127
       Thread(s) per core:    2
       Core(s) per socket:    16
       Socket(s):             4
```

(Continued on next page)

Cisco Systems

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SPECrate2017_fp_peak =   372

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

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Platform Notes (Continued)

```
        NUMA node(s):            8
        Vendor ID:              GenuineIntel
        CPU family:             6
        Model:                  85
        Model name:             Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
        Stepping:               4
        CPU MHz:                2290.236
        CPU max MHz:            3700.0000
        CPU min MHz:            1000.0000
        BogoMIPS:               5199.98
        Virtualization:         VT-x
        L1d cache:              32K
        L1i cache:              32K
        L2 cache:               1024K
        L3 cache:               22528K
        NUMA node0 CPU(s):      0-3,8-11,64-67,72-75
        NUMA node1 CPU(s):      4-7,12-15,68-71,76-79
        NUMA node2 CPU(s):      16-19,24-27,80-83,88-91
        NUMA node3 CPU(s):      20-23,28-31,84-87,92-95
        NUMA node4 CPU(s):      32-35,40-43,96-99,104-107
        NUMA node5 CPU(s):      36-39,44-47,100-103,108-111
        NUMA node6 CPU(s):      48-51,56-59,112-115,120-123
        NUMA node7 CPU(s):      52-55,60-63,116-119,124-127
        Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
    dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
    vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid
    rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
    avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 22528 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 8 nodes (0-7)
    node 0 cpus: 0 1 2 3 8 9 10 11 64 65 66 67 72 73 74 75
    node 0 size: 191934 MB
    node 0 free: 191713 MB
    node 1 cpus: 4 5 6 7 12 13 14 15 68 69 70 71 76 77 78 79
    node 1 size: 193528 MB
    node 1 free: 193331 MB
    node 2 cpus: 16 17 18 19 24 25 26 27 80 81 82 83 88 89 90 91
```

(Continued on next page)

Cisco Systems

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SPECrate2017_fp_peak =   372

CPU2017 License: 9019
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Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```
   node 2 size: 193528 MB
   node 2 free: 193325 MB
   node 3 cpus: 20 21 22 23 28 29 30 31 84 85 86 87 92 93 94 95
   node 3 size: 193528 MB
   node 3 free: 193351 MB
   node 4 cpus: 32 33 34 35 40 41 42 43 96 97 98 99 104 105 106 107
   node 4 size: 193528 MB
   node 4 free: 193326 MB
   node 5 cpus: 36 37 38 39 44 45 46 47 100 101 102 103 108 109 110 111
   node 5 size: 193528 MB
   node 5 free: 193319 MB
   node 6 cpus: 48 49 50 51 56 57 58 59 112 113 114 115 120 121 122 123
   node 6 size: 193528 MB
   node 6 free: 193351 MB
   node 7 cpus: 52 53 54 55 60 61 62 63 116 117 118 119 124 125 126 127
   node 7 size: 193525 MB
   node 7 free: 193318 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  21  21
     1:  11  10  21  21  21  21  21  21
     2:  21  21  10  11  21  21  21  21
     3:  21  21  11  10  21  21  21  21
     4:  21  21  21  21  10  11  21  21
     5:  21  21  21  21  11  10  21  21
     6:  21  21  21  21  21  21  10  11
     7:  21  21  21  21  21  21  11  10

 From /proc/meminfo
   MemTotal:       1583749960 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
   SuSE-release:
     SUSE Linux Enterprise Server 12 (x86_64)
     VERSION = 12
     PATCHLEVEL = 2
     # This file is deprecated and will be removed in a future service pack or release.
     # Please check /etc/os-release for details about this release.
   os-release:
     NAME="SLES"
     VERSION="12-SP2"
     VERSION_ID="12.2"
     PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
     ID="sles"
     ANSI_COLOR="0;32"
```

(Continued on next page)

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Platform Notes (Continued)

```
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Dec 31 23:43

 SPEC is set to: /opt/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sda1       xfs   280G   77G  203G  28% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
   Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
  CC  519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CC  519.lbm_r(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
  CXXC 508.namd_r(base) 510.parest_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
```

(Continued on next page)

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SPECrate2017_fp_base = 364

SPECrate2017_fp_peak = 372

Compiler Version Notes (Continued)

```
CXXC 508.namd_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CC   511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
CC   511.povray_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC   507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC   503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
FC   554.roms_r(peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
```

(Continued on next page)

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Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------

==========================================================================
  CC   521.wrf_r(base) 527.cam4_r(base)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------

==========================================================================
CC   521.wrf_r(peak) 527.cam4_r(peak)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
`icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`

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Base Portability Flags (Continued)

507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

C++ benchmarks:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both C and C++:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

538.imagick_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

544.nab_r: `Same as 538.imagick_r`

C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

(Continued on next page)

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https://www.spec.org/

Cisco Systems

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2.60 GHz)

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SPECrate2017_fp_peak = 372

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Peak Optimization Flags (Continued)

510.parest_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:

503.bwaves_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3 -auto`
`-nostandard-realloc-lhs`

549.fotonik3d_r: `Same as 503.bwaves_r`

554.roms_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3`
`-no-prec-div -qopt-prefetch -ffinite-math-only`
`-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:
`-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3`
`-no-prec-div -qopt-prefetch -ffinite-math-only`
`-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both C and C++:

511.povray_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX2 -O3`
`-no-prec-div -qopt-prefetch -ffinite-math-only`
`-qopt-mem-layout-trans=3`

526.blender_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only`
`-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC CPU2017 Floating Point Rate Result

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Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECrate2017_fp_base =   364

SPECrate2017_fp_peak =   372

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-11-05 18:31:14-0500.
Report generated on 2018-11-27 13:38:29 by CPU2017 PDF formatter v6067.
Originally published on 2018-11-27.