SPEC® CFP2006 Result
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ScaleMP

vSMP Foundation with PowerEdge M610
(Intel Xeon X5570, 2.93 GHz)

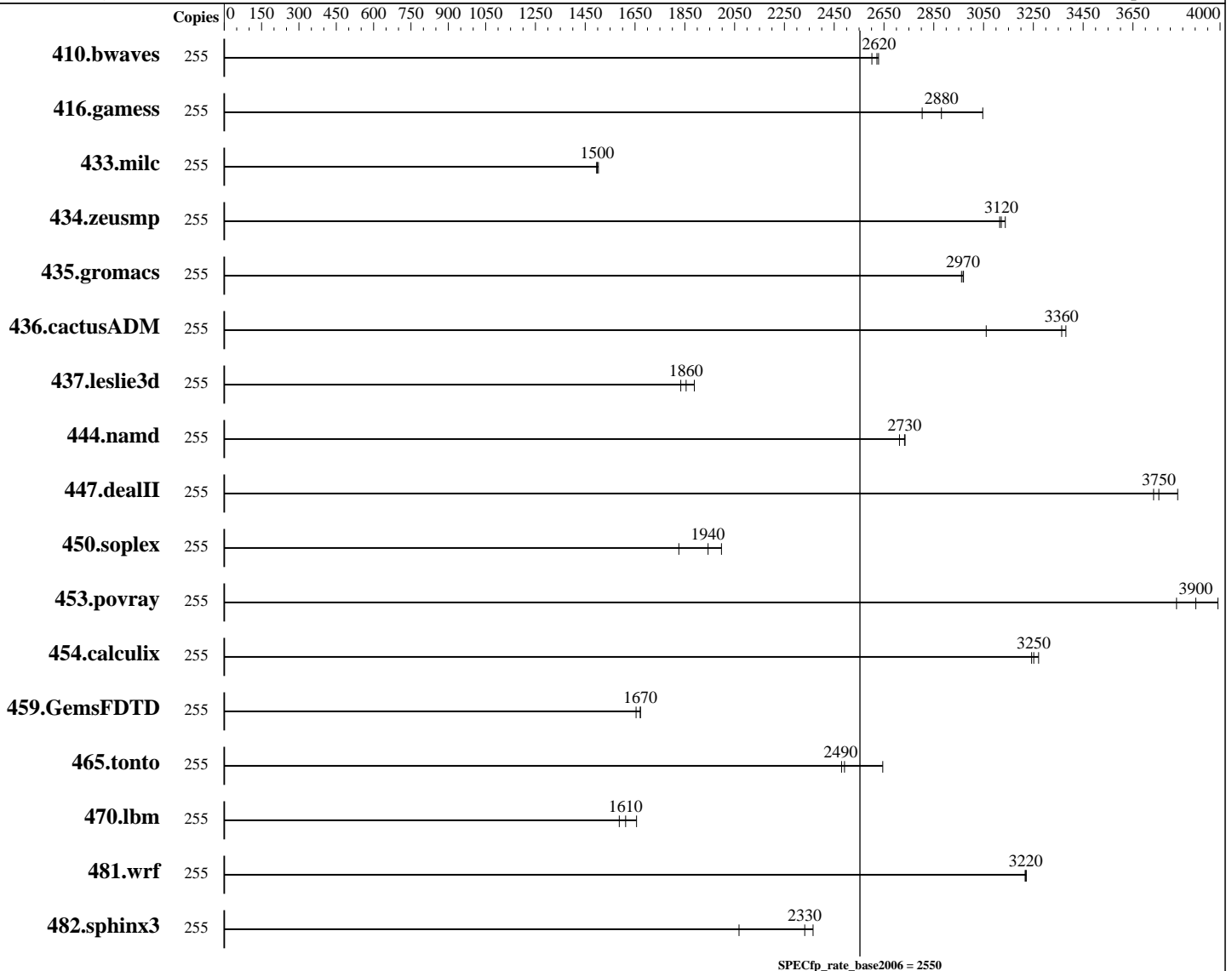$SPECfp®_rate2006 = $ Not Run

$SPECfp_rate_base2006 = $ 2550

CPU2006 license: 2929	**Test date:** Aug-2009
Test sponsor: ScaleMP	**Hardware Availability:** Apr-2009
Tested by: ScaleMP	**Software Availability:** Apr-2009

Benchmark	Copies	Result
410.bwaves	255	2620
416.gamess	255	2880
433.milc	255	1500
434.zeusmp	255	3120
435.gromacs	255	2970
436.cactusADM	255	3360
437.leslie3d	255	1860
444.namd	255	2730
447.dealII	255	3750
450.soplex	255	1940
453.povray	255	3900
454.calculix	255	3250
459.GemsFDTD	255	1670
465.tonto	255	2490
470.lbm	255	1610
481.wrf	255	3220
482.sphinx3	255	2330

SPECfp_rate_base2006 = 2550

Hardware

CPU Name:	Intel Xeon X5570
CPU Characteristics:	Intel Turbo Boost Technology is not-enabled
CPU MHz:	2933
FPU:	Integrated
CPU(s) enabled:	128 cores, 32 chips, 4 cores/chip, 2 threads/core
CPU(s) orderable:	8,16,24,32,40,48,56,64,96,128 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core

Continued on next page

Software

Operating System:	Red Hat Enterprise Linux Server release 5.3 (Tikanga) Kernel: 2.6.21.7-16.vSMP.nomc
Compiler:	Intel C++ and Fortran Compiler 11.0 for Linux Build 20081105 Package ID: l_cproc_p_11.0.074, l_fproc_p_11.0.074
Auto Parallel:	No
File System:	xfs
System State:	Multi-user, run level 3

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L3 Cache:	8 MB I+D on chip per chip
Other Cache:	92 GB I+D off chip per system
Memory:	768 GB (16 x 2 x 6 x 4 GB DDR3-1066R, ECC, CL9)
Disk Subsystem:	16 x 160 GB SATA, 7200 RPM
Other Hardware:	None

Base Pointers:	64-bit
Peak Pointers:	Not Applicable
Other Software:	ScaleMP vSMP Foundation 2.0.65.35

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
410.bwaves	255	**1322**	**2620**	1319	2630	1332	2600							
416.gamess	255	1639	3050	**1733**	**2880**	1781	2800							
433.milc	255	1565	1500	1557	1500	**1562**	**1500**							
434.zeusmp	255	**743**	**3120**	740	3140	745	3110							
435.gromacs	255	615	2960	613	2970	**613**	**2970**							
436.cactusADM	255	996	3060	**906**	**3360**	901	3380							
437.leslie3d	255	**1292**	**1860**	1269	1890	1307	1830							
444.namd	255	754	2710	748	2730	**748**	**2730**							
447.dealII	255	762	3830	**777**	**3750**	781	3730							
450.soplex	255	1165	1830	1065	2000	**1094**	**1940**							
453.povray	255	355	3830	**348**	**3900**	340	3990							
454.calculix	255	643	3270	649	3240	**647**	**3250**							
459.GemsFDTD	255	**1619**	**1670**	1619	1670	1635	1650							
465.tonto	255	949	2650	1012	2480	**1007**	**2490**							
470.lbm	255	2116	1660	**2173**	**1610**	2208	1590							
481.wrf	255	885	3220	884	3220	**885**	**3220**							
482.sphinx3	255	2101	2370	2404	2070	**2131**	**2330**							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
   The config file option 'submit' was used.
     numactl was used to bind copies to the cores
```

Platform Notes

```
     ScaleMP
       vSMP Foundation: 2.0.65.35
     Other Cache:
       ScaleMP vSMP Foundation manages cache coherency between the
       InfiniBand-connected systems via multiple concurrent memory
       coherency mechanisms, on a per-block basis, based on
       real-time memory activity access patterns.
       This mechanism reserves 92 GB of the main memory across all
       boards (distributed), which is used as a 4th level cache.
```

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Platform Notes (Continued)

```
    Hardware Details:
        System was aggregated using 16 X Dell PowerEdge M610.
        The servers were connected with Melanox InfiniBand QDR and a
        QDR switch.
    CPU Characteristics: Intel Turbo Boost Technology not-enabled:
        As the prerequisites listed below for enablement of this
        technology did not exist.
        The prerequisites for Turbo Boost Technology are:
        - Hardware: Enabling Turbo Boost Technology require BIOS setting.
        - Software: OS needs to be ACPI-aware and set P0 power state.
```

Base Compiler Invocation

C benchmarks:
```
    icc
```

C++ benchmarks:
```
    icpc
```

Fortran benchmarks:
```
    ifort
```

Benchmarks using both Fortran and C:
```
    icc ifort
```

Base Portability Flags

```
      410.bwaves: -DSPEC_CPU_LP64
      416.gamess: -DSPEC_CPU_LP64
        433.milc: -DSPEC_CPU_LP64
      434.zeusmp: -DSPEC_CPU_LP64
     435.gromacs: -DSPEC_CPU_LP64 -nofor_main
   436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
      437.leslie3d: -DSPEC_CPU_LP64
        444.namd: -DSPEC_CPU_LP64
       447.dealII: -DSPEC_CPU_LP64
       450.soplex: -DSPEC_CPU_LP64
      453.povray: -DSPEC_CPU_LP64
     454.calculix: -DSPEC_CPU_LP64 -nofor_main
   459.GemsFDTD: -DSPEC_CPU_LP64
       465.tonto: -DSPEC_CPU_LP64
        470.lbm: -DSPEC_CPU_LP64
         481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
     482.sphinx3: -DSPEC_CPU_LP64
```

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Base Optimization Flags

C benchmarks:
    -xSSE4.2 -ipo -O3 -no-prec-div -static

C++ benchmarks:
    -xSSE4.2 -ipo -O3 -no-prec-div -static

Fortran benchmarks:
    -xSSE4.2 -ipo -O3 -no-prec-div -static

Benchmarks using both Fortran and C:
    -xSSE4.2 -ipo -O3 -no-prec-div -static

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic11.0-fp-linux64-revE.20090710.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic11.0-fp-linux64-revE.20090710.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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